WHAT IS CLAIMED IS:

1. A storage device, comprising:

two random access memories each having at least 2^{N-1} locations for storing data at respective addresses, N being an integer greater than 1, a data input connected to a data source, a command input, an address input and an output;

multiplexing means having first and second data inputs respectively connected to the data outputs of the two memories, a third data input connected to the data source and an output reproducing data present at one of said first, second and third data inputs, selected by switching signals;

a controller for issuing electrical signals, within successive time intervals, on controller's outputs including two access command outputs respectively connected to the command inputs of the two memories, two address outputs respectively connected to the address inputs of the two memories and at least a switching command output for issuing said switching signals; and

means for sampling the output of the multiplexing means at the beginning of each time interval and producing output data of the device,

wherein the controller is set up for issuing, in the course of two consecutive sequences of 2^N time intervals:

on each of the two access command outputs, and for at least time intervals distinct from the boundaries of the two sequences, alternate read and write access commands, a write access command being issued on one of said access command outputs while a read access command is issued on the other access command output and vice versa;

on each of the two address outputs, increasing addresses during one of the two sequences and decreasing addresses during the other sequence, such that, for at least time intervals distinct from the boundaries of the two sequences, the address input of each memory receives the same address in the course of two consecutive time intervals of each sequence during which the command input of said memory receives a read access command and then a write access command; and

on each switching command output, switching signals set so that in the course of each sequence, the sampling means produce data originating from the source in a reverse chronological order from the chronological order of arrival of said data from the source.

2. The device according to Claim 1, wherein, during at least one time interval at a boundary of each sequence, the switching signals are issued so that the output of the multiplexing means reproduces data present at said third data input.

3. The device according to Claim 1, wherein the controller is set up for coding the addresses of each memory over N-1 bits

4. The device according to Claim 1, wherein the means for sampling the output of the multiplexing means include a flip-flop D.

5. The device according to Claim 1, wherein the two memories are deferred read memories, the data read in each memory being produced at the output of said memory during the time interval immediately following the time interval during which the command input of said memory receives a read access command and the address input of said memory receives an address.

6. The device according to Claim 1, wherein the multiplexing means include:

a first multiplexer having:

a switching command input connected to a first switching command output of the controller,

first and a second data inputs connected respectively to the outputs of the two memories, and

an output reproducing the signals from the first or second input of said first multiplexer according to a first switching signal applied to the command input of said first multiplexer; and

a second multiplexer having:

a switching command input connected to a second switching command output of the controller,

first and second data inputs connected respectively to the data source and to the output of the first multiplexer, and

an output reproducing the signals from the first or second input of said second multiplexer according to a second switching signal applied to the command input of said second multiplexer.

7. The device according to Claim 6, wherein the controller is set up so that the first switching signal and the access command issued by the controller to one of the two memories are identical binary signals, for at least time intervals distinct from the boundaries of the two sequences.

8. The device according to Claim 6, wherein the two memories are deferred read memories, the data read in each memory being produced at the output of said memory during the time interval immediately following the time interval during which the command input of said memory receives a read access command and the address input of said memory receives an address, and wherein the controller comprises:

a cyclic counter of the time intervals of the two consecutive sequences, set up to produce a number over N+1 bits, between 0 and $2^{N+1}-1$, for counting the time interval in progress;

means for generating at a first access command output connected to a first of the two memories a first binary access command opposite to the least significant bit of the count number of the time interval in progress,

during the time intervals respectively numbered from 0 to 2^N-3 and from 2^N to $2^{N+1}-3$;

means for generating the second access command at a second access command output connected to the second of the two memories in the form of the least significant bit of the count number of the time interval in progress, during the time intervals respectively numbered from 0 to 2^N-2 and from 2^N to $2^{N+1}-2$;

means for producing, during each time interval, a first partial time interval count number over N-1 bits, equal to the count number for the time interval in progress from which the most significant bit and the least significant bit have been removed;

means for generating at a first address output connected to the address input of said first memory an address equal to the first partial count number during the time intervals respectively numbered from 0 to 2^N-3, and equal to $2^{N-1}-2$ from which the first partial count number is subtracted during the time intervals respectively numbered from 2^N to $2^{N+1}-3$;

means for producing, during each time interval, a second partial time interval count number over N-1 bits, equal to the count number for the time interval in progress

to which 1 is added, then from which the most significant bit and the least significant bit have been removed;

means for generating at a second address output connected to the address input of said second memory an address equal to the second partial count number during the time intervals respectively numbered from 0 to 2^N-2, and equal to 2^{N-1}-1 from which the second partial count number is subtracted during the time intervals respectively numbered from 2^N to 2^{N+1}-2;

means for generating at the first switching command output the first switching signal in the form of a binary signal opposite to said first access command;

means for generating at the second switching command output the second switching signal in the form of a binary signal equal to 1 when the count number for the time interval in progress, reduced to the N least significant bits, is equal to 2^N-1, and equal to 0 otherwise;

each of the two memories being in write or read access mode when the corresponding access command is equal to 0 or 1, respectively;

the first and second multiplexer each being set up to instantaneously reproduce at the output of said

multiplexer a signal applied to the first or second input of said multiplexer, when the switching signal applied to the command input of said multiplexer is equal to 0 or 1, respectively.

9. The device according to Claim 8, wherein:

the means of the controller for generating the first access command are set up to produce, during each time interval, a binary signal opposite to the least significant bit of the count number for the time interval in progress;

the means of the controller for generating an address at said first address output are set up to produce an address equal to the first partial count number during the time intervals respectively numbered from 0 to 2^N-1, and equal to 2^{N-1}-2 from which the first partial count number is subtracted during the time intervals respectively numbered from 2N to

2^{N+1}-1;

the means of the controller for generating the second access command are set up to produce, during each time interval, a signal equal to the least significant bit of the time interval in progress; and

the means of the controller for generating an address at said second address output are set up to produce an address equal to the second partial count number during the time intervals respectively numbered from 0 to 2^N-2 or numbered 2^{N+1}-1, and equal to 2^{N-1}-1 from which the second partial count number is subtracted during the time intervals respectively numbered from 2^N to 2^{N+1}-1, or numbered 2^N-1.

10. The device according to Claim 9, wherein the controller comprises:

a first internal multiplexer having a first input connected to receive the first partial count number, a second input connected to receive the value, over N-1 bits, of 2^{N-1}-2 from which the first partial count number is subtracted, a command input connected to receive the most significant bit of the count number for the time interval in progress, and set up to reproduce at an output connected to the first address output of the controller the value received on the first or second input of said first internal multiplexer, when the value applied to the command input of said first internal multiplexer is 0 or 1, respectively; and

a second internal multiplexer having a first input connected to receive the second partial count number, a second input connected to receive the value, over N-1 bits, of $2^{N-1}-1$ from which the second partial count number is subtracted, a command input connected to receive the most significant bit of the count number for the time interval in progress to which 1 is added, and set up to reproduce at an output connected to the second address output of the controller the value received at the first or second input of said second internal multiplexer, when the value applied to the command input of said second internal multiplexer is 0 or 1, respectively.

11. The device according to Claim 6, wherein the memories are instant read memories, the data read in each memory being produced at the output of said memory in the time interval during which the command input of said memory receives a read access command and the address input of said memory receives an address, and wherein the controller comprises:

a cyclic counter of the time intervals of the two consecutive sequences, set up to produce a number over N+1

bits, between 0 and $2^{N+1}-1$, for counting the time interval in progress;

means for producing, during each time interval, a first partial time interval count number over N-1 bits, equal to the count number for the time interval in progress from which the most significant bit and the least significant bit have been removed;

means for producing, during each interval, a second partial time interval count number over N-1 bits, equal to the count number for the time interval in progress to which 1 is added, then from which the most significant bit and the least significant bit have been removed;

means for generating at said second switching command output the second switching signal in the form of a binary signal equal to 0 when the count number for the time interval in progress, reduced to the N least significant bits, is equal to 2^N-1, and equal to 1 otherwise;

means for generating at a first address output connected to the address input of a first of the two memories an address equal to the first partial count number during the time intervals respectively numbered from 0 to 2^N-2, and equal to $2^{N-1}-1$ from which the second partial

count number is subtracted during the time intervals respectively numbered from 2^N to $2^{N+1}-2$;

means for generating at a second address output connected to the address input of a second of the two memories an address equal to the second partial count number during the time intervals respectively numbered from 0 to 2^N-2, and equal to $2^{N-1}-1$ from which the first partial count number is subtracted during the time intervals respectively numbered from 2^N to $2^{N+1}-2$;

means for generating at a first access command output connected to said first memory a first binary access command, for the time intervals numbered other than 2^N-1 and $2^{N+1}-1$, equal to:

$[^{C}C(0)$ EXCL_OR $C(N)]$ OR ^{C}[second switching signal],

where:

C(0) is the least significant bit of the time interval in progress,

C(N) is the most significant bit of the time interval in progress,

EXCL_OR is the "exclusive OR" binary operator,

^{C}X designates the opposite value to the binary value X;

means for generating at the second access command output connected to said second memory a second binary

access command equal to [C(0) EXCL_OR C(N)] OR ^{C}[second switching signal], for the time intervals respectively numbered other than 2^{N}-1 and 2^{N+1}-1;

means for generating at the first switching command output a binary signal opposite to the first access command;

each of the two memories being in write or read access mode when the corresponding access command is equal to 0 or 1, respectively;

the first and second multiplexer each being set up to instantaneously reproduce at the output of said multiplexer a signal applied to the first or second input of said multiplexer, when the switching signal applied to the command input of said multiplexer is equal to 0 or 1, respectively.

12. The device according to Claim 11, wherein:

the means of the controller for generating the first access command are set up to produce, during each time interval, a binary signal equal to [^{C}C(0) EXCL_OR C(N)];

the means of the controller for generating the second access command are set up to produce, during each

time interval, a binary signal opposite to the first access command;

the means for generating an address at the first address output are set up to produce a signal equal to the first partial count number during the time intervals respectively numbered from 0 to 2^N-1, and equal to 2^{N-1}-1 from which the second partial count number is subtracted during the time intervals respectively numbered 2^N to 2^{N+1}-1;

the means for generating an address at the second address output are set up to produce a signal equal to the second partial count number during the time intervals respectively numbered from 0 to 2^N-1, and equal to 2^{N-1}-1 from which the first partial count number is subtracted during the time intervals respectively numbered 2^N to 2^{N+1}-1.

13. The device according to Claim 12, wherein the controller comprises:

a first internal multiplexer having a first input connected to receive the first partial count number, a second input connected to receive the value, over N-1 bits, of 2^{N-1}-1 from which the second partial count number is

subtracted, a command input connected to receive the most significant bit of the count number for the time interval in progress, and set up to reproduce at an output connected to the first address output of the controller the value received at the first or second input of said first internal multiplexer, when the value applied to the command input of said first internal multiplexer is 0 or 1, respectively; and

a second internal multiplexer having a first input connected to receive the second partial count number, a second input connected to receive the value, over N-1 bits, of 2^{N-1}-1 from which the first partial count number is subtracted, a command input connected to receive the most significant bit of the count number for the time interval in progress, and set up to reproduce at an output connected to the second address output of the controller the value received at the first or second input of said second internal multiplexer, when the value applied to the command input of said second internal multiplexer is 0 or 1, respectively.

14. The device according to Claim 1, wherein the memories are instant read memories, the data read in each

memory being produced at the output of said memory in the time interval during which the command input of said memory receives a read access command and the address input of said memory receives an address.

15. A method of data storage comprising the following steps each carried out within successive time intervals of two consecutive sequences of 2N time intervals, N being an integer greater than 1:

issuing a data from a data source to two random access memories, each memory having at least 2N-1 locations for storing data at respective addresses, while issuing directly said data to a multiplexer further connected to respective data outputs of the two memories;

for at least time intervals distinct from the boundaries of the two sequences, issuing alternate read and write access commands respectively to each of the two random access memories, a write access command being issued to one of the memories while a read access command is issued to the other memory and vice versa;

issuing to each memory, increasing addresses during one of the two sequences and decreasing addresses during the other sequence, such that, for at least time intervals distinct from boundaries of the two sequences, each memory receives the same address in the course of two consecutive time intervals of each sequence during which

said memory receives a read access command and then a write access command; and

issuing switching signals to the multiplexer, the switching signals causing the multiplexer to reproduce on an output either the data received directly from the data source or the data received from one of the two memories, as selected by the switching signals, so that in the course of each sequence, data is produced which originates from the source in a reverse chronological order from the chronological order of arrival of said data from the source.

16. A data storage device, comprising:

two random access memories for storing data at respective addresses, a data input connected to a data source, a command input, an address input and an output;

a multiplexor having first and second data inputs respectively connected to the data outputs of the two memories and an output reproducing data present at one of said first and second data inputs;

a controller for issuing command signals to the command inputs of the two memories, address signals to the address inputs of the two memories and switching signals to the multiplexor; and

a logic device to sample the output of the multiplexor and produce output data,

wherein the controller issues:

alternate read/write command signals to the two random access memories so as to write data to one memory while reading data from another memory;

address signals to the address inputs of the two random access memories, while alternate read/write command signals are provided, comprising increasing address values followed by decreasing address values; and

switching signals to the multiplexor to alternately select between the two random access memories with respect to data read from the memories.

17. The data storage device of claim 16 further comprising:

a second multiplexor having first and second data inputs respectively connected to the outputs of the first multiplexor and a source of data and an output reproducing data present at one of said first and second data inputs;

wherein the controller issues switching signals to the second multiplexor to selectively output data received from the source of data instead of data received from the multiplexor.

18. A method for LIFO data storage comprising:

alternately writing received data into first and second memories;

oppositely alternately reading previously written data from the first and second memories; and

selecting addresses in the first and second memories for the writing/reading of data to sequentially increment through the memories during a first time interval and then sequentially decrement through the memories during an immediately following second time interval.

19. The method of claim 18 wherein the selection of addresses selects an address in one of the memories in the first time interval for writing data into the memory and then selects the same address in the same one of the memories in the second time interval for reading data from the memory.

20. The method of claim 18 wherein the oppositely alternatively reading includes alternately selecting between the first and second memories to output read data.

21. The method of claim 20 wherein the output read data is produced in a reverse chronological order to that with which it was received.